

IN THE DRAWINGS

Please replace FIG. 1 with the enclosed replacement drawing for FIG.1. An annotated drawing shows changes shown by red ink. Specifically, "nFEO" is replaced with "nREO" and "FS[1:0]" is replaced with "FS[7:0]".

REMARKS

Claims 1-4, and 6-32 are pending in the application.

Claims 5, 6 and 9 are cancelled.

Claims 31 and 32 are allowed.

Claims 1-4, 6-18 and 21-30 are rejected.

Claims 19 and 20 are objected to.

Claims 1-4, 6-18 and 21-26 are rejected under 35 U.S.C. 103(a).

Claims 27-30 are rejected under 35 U.S.C. 103(a).

Claims 1, 8, 21 and 27 are currently amended.

Claims 33 and 34 are new.

No new matter is added.

Claims 1-4, 7, 8 and 10-34 remain in the case for consideration.

Applicant requests reconsideration and allowance of the claims in light of the above amendments and following remarks.

Informalities

Amendments to the Specification text and FIG. 1 repair clerical errors. No new matter is introduced.

Claim Objections

Applicant is advised that should claim 9 be found allowable, claim 10 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof.

Claim 9 has been cancelled. Withdrawal of the objection is requested.

Claim 6 is objected to in the Office Action mailed February 25, 2005.

Claim 6 has been amended to address the objection. Withdrawal of the objection is requested.

Claim Rejections – 35 U.S.C. § 103

Claims 1-4, 6-18 and 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raad, et al. (6,243,840 and "Raad" hereinafter) in view of Hill, et al. (6,141,779 and "Hill" hereinafter).

The applicant respectfully traverses the rejections.

Claim 1 has been amended to recite “a data output buffer adapted to operate in a first mode and a second mode, wherein the first mode operates to output for outputting data stored in the memory cells; a comparator to determine failure of the memory cells to store the data, by comparing the stored data with expected data; and a fail bit counter for counting the number of those of the memory cells that fail to store data, and for outputting a fail code representing the counted number of the fail bits to the data output buffer, wherein the second mode of the data output buffer operates to output the fail code.” No new matter is added. Support can be found on page 9, lines 5-15, FIGS. 1 and 7, among other locations. Using a single data output buffer for both normal output data and a test result's fail code is advantageous in that space and the number of external pin connections can be reduced in a semiconductor package. For example, the same pins can be used for normal output data as for fail code data.

In contrast, neither Raad nor Hill disclose a data output buffer that is adapted to operate in two modes, as recited in claim 1. Raad does not teach the fail bit counter, as the Examiner has previously noted, let alone a fail code. Hill, as well, does not teach a data output buffer as recited in claim 1. Hill shows, in FIG 3, a counter (144) that outputs an encoded RAM redundancy map value to a nonvolatile storage (146). This, in fact, teaches away from claim 1 because the output value from the counter (144) does not represent a fail code that can be transmitted by the same data output buffer that can transmit the cell array data (104). For these reasons, the cited references, either alone or in combination, do not teach or suggest all of the limitations of claim 1. Accordingly, the applicant asserts that the rejection does not present a *prima facie* case of obviousness, and claim 1 is allowable.

Claims 2-4 and 7 depend from claim 1 and inherently include all of the limitations of the base claim. As discussed above, the prior art does not teach the limitations of the base claim much less the further embodiments of the dependent claims. Therefore, claims 2-4 and 7 are allowable for their dependency and their own merits. Allowance of these claims is requested.

Claim 8 has been amended to recite “a data output buffer adapted to operate in a first mode and a second mode, wherein the first mode operates to output data stored in the memory cells and the second mode operates to output the fail code.” No new matter is added. Support can be found on page 9, lines 5-15, FIGS. 1 and 7, among other locations. For the same reasons described above regarding claim 1, the applicants assert that the cited references, either alone or in combination, do not teach or suggest all of the limitations of

claim 8. Accordingly, the rejection does not present a *prima facie* case of obviousness, and claim 8 is allowable.

Claims 10-18 depend from claim 8 and inherently include all of the limitations of the base claim. As discussed above, the prior art does not teach the limitations of the base claim much less the further embodiments of the dependent claims. Therefore, claims 10-18 are allowable for their dependency and their own merits. Allowance of these claims is requested.

Claim 21 has been amended to recite "*outputting data stored in the memory cells from a data output buffer; and outputting the fail code from the data output buffer.*" No new matter has been added. Support can be found as explained regarding claims 1 and 8. Also, for the same reasons described above regarding claim 1, the applicants assert that the cited references, either alone or in combination, do not teach or suggest all of the limitations of claim 21. Accordingly, the rejection does not present a *prima facie* case of obviousness, and claim 21 is allowable.

Claims 22-26 depend from claim 21 and inherently include all of the limitations of the base claim. As discussed above, the prior art does not teach the limitations of the base claim much less the further embodiments of the dependent claims. Therefore, claims 22-26 are allowable for their dependency and their own merits. Allowance of these claims is requested.

Claims 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raad, et al. (6,243,840 and "Raad" hereinafter) in view of Hill, et al. (6,141,779 and "Hill" hereinafter) and Beffa, et al. (6,032,264 and "Beffa" hereinafter).

The applicant respectfully traverses the rejection.

Claim 27 has been amended to recite "*outputting data stored in the memory cells from a data output buffer; and outputting the fail code from the data output buffer.*" No new matter has been added. Support can be found as explained regarding claims 1 and 8. Also, for the same reasons described above regarding claim 1, the applicants assert that the cited references, either alone or in combination, do not teach or suggest all of the limitations of claim 27. Accordingly, the rejection does not present a *prima facie* case of obviousness, and claim 27 is allowable.

Claims 28-30 depend from claim 27 and inherently include all of the limitations of the base claim. As discussed above, the prior art does not teach the limitations of the base claim much less the further embodiments of the dependent claims. Therefore, claims 28-30 are allowable for their dependency and their own merits. Allowance of these claims is requested.

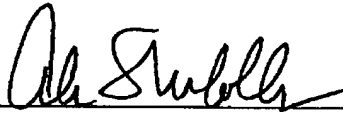
Allowable Subject Matter

As recited in the office action mailed February 25, 2005, claims 31 and 32 are allowable.

For the foregoing reasons, reconsideration and allowance of claims 1-4, 7, 8 and 10-34 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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NONVOLATILE SEMICONDUCTOR MEMORY DEVICE WITH A FAIL BIT DETECTING SCHEME AND METHOD FOR COUNTING THE NUMBER OF FAIL BITS

Attorney Docket No. 4590-220/Application No. 10/003,390

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Annotated Sheet Showing Changes

Fig. 1

